Turn-around time reduction for 3DIC Timing signoff

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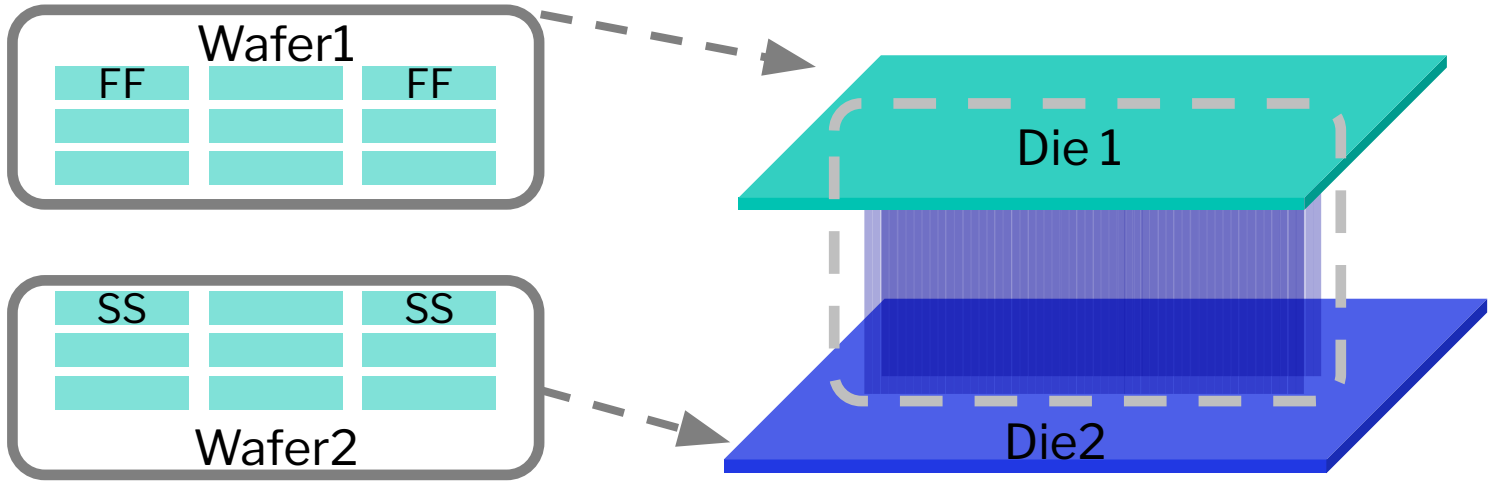
3DIC STA Sign-off Objective

- 3DIC STA sign-off is how to consider Die to Die variation
  - 3DIC has dies which was in different wafers or lots
  - To consider die to die variation, we need to increase sign-off corners such as a SS+FF corner
    - It increases turn-around time and computing resource



Why We Reduce Timing Sign-off Corner

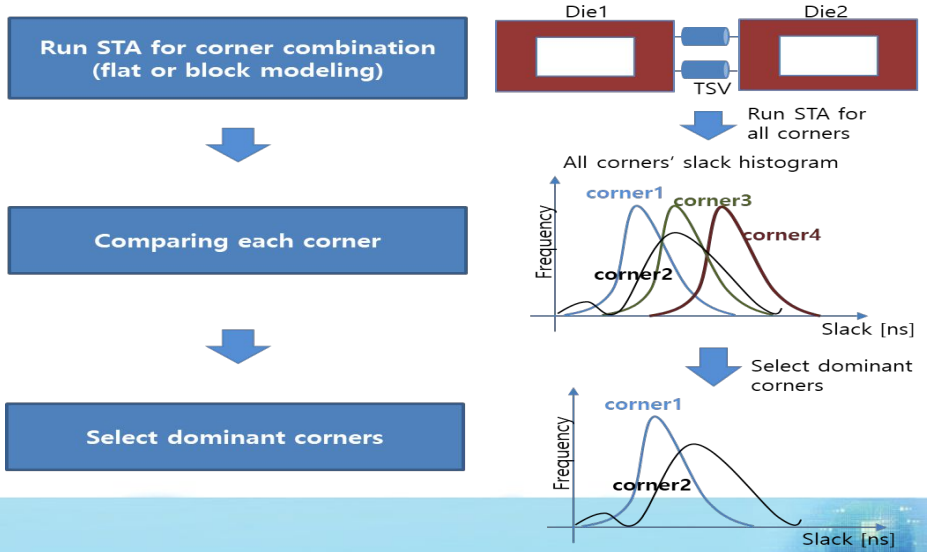
- Increased sign-off corner makes Turn-around time be increased
  - Example: 3DIC sign-off corner is combination of single die's sign-off corners

Die1 PVT	Die2 PVT	Default
4 corners: SS_Vmin_cold_Cmax SS_Vmin_hot_Cmax FF_Vmax_cold_Cmin FF_Vmax_hot_Cmin	4 corners: SS_Vmin_cold_Cmax SS_Vmin_hot_Cmax FF_Vmax_cold_Cmin FF_Vmax_hot_Cmin	16 corners (4x4 corners)

  - There are three methods
    - Making asynchronous interface scheme
    - Sign-off for dominant corners based on the target design characteristic
    - Budget based sign-off

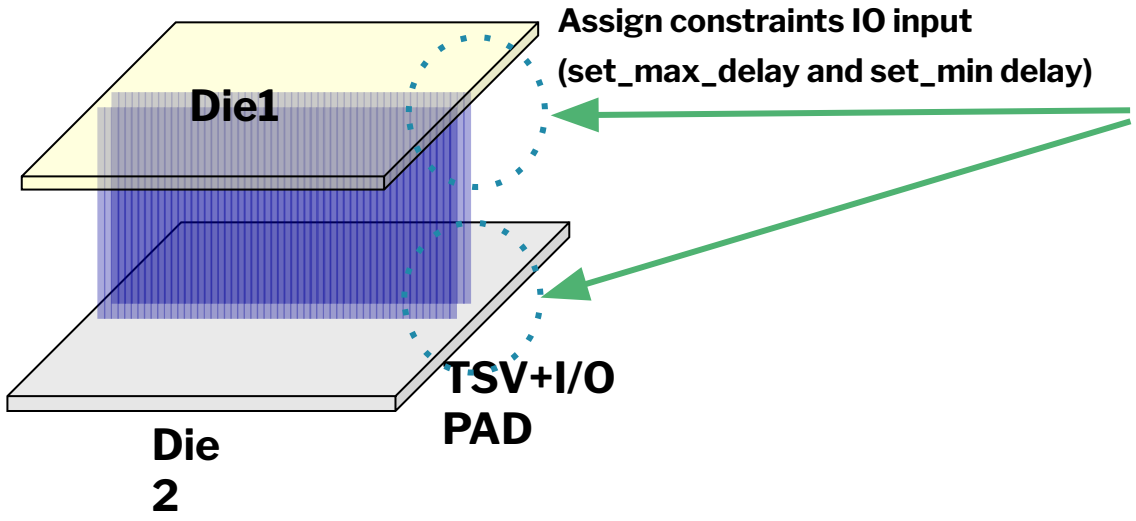
3DIC Sign-off Corner Reduction Method 1

- Dominant corner analysis method
  - Using ubumps, we make simple R2R interface
  - For simple R2R path, one or two corners cover all other sign-off corners
    - They are dominants corners
  - After finding dominant corners, we can do sign-off for the dominant corners
  - This method can reduce the sing corner dramatically



3DIC Sign-off Corner Reduction Method 2

- Budget based sign-off method
  - Each die does the sign-off itself The paths in the die are covered by single die
  - If we can make budgeted constraint for each die' IO, we can do separated sign-off foe each dies



Budget-based Flow

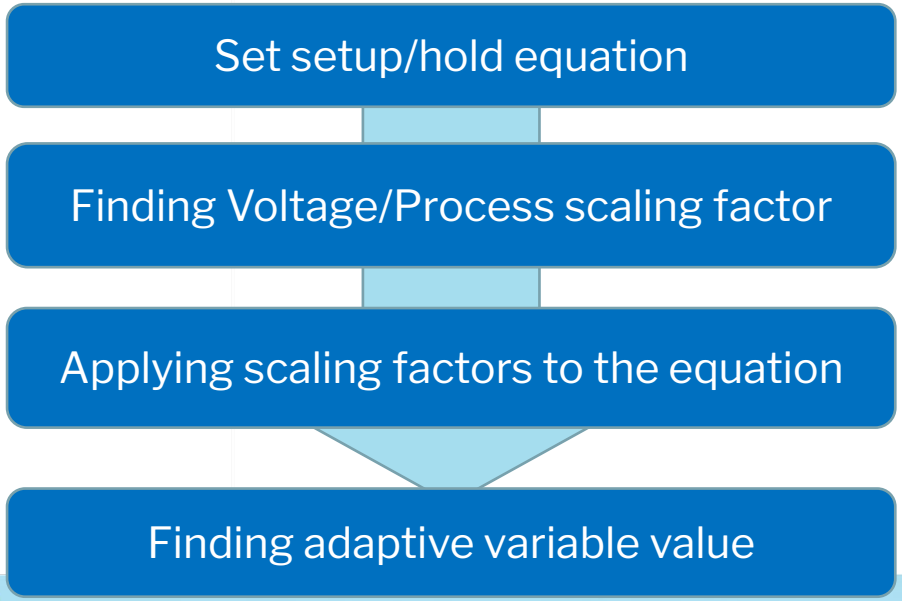
[Constraint Budgeting]
1) Tier1: set delay constraints on register-to-IO input paths
2) TSV: IO-to-IO Path
3) Tier2 : set delay constraints IO-to-register paths

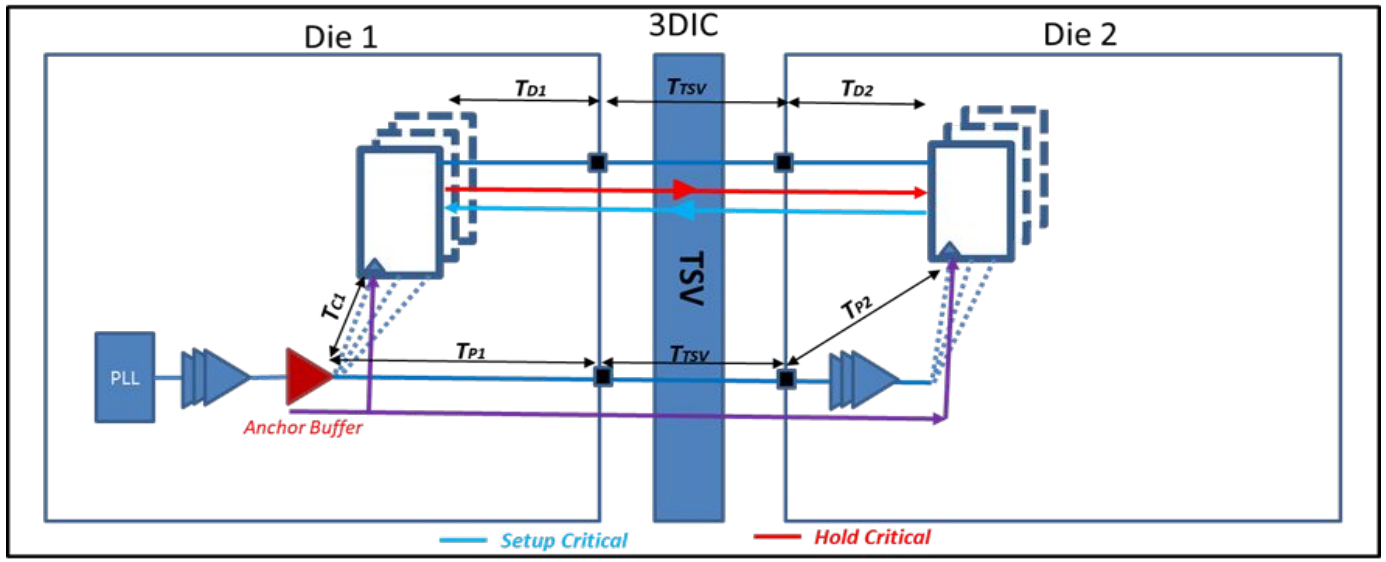
Add the constraints and run STA

Run SPICE simulation using TSV paths and check the constraints

3DIC Sign-off Corner Reduction Method 3-1

- Constraint budgeting method with estimation
  - If we estimate stage delay in the path, we can reduce the overhead for budgeting method
    - If we don't know stage delay, we should have large uncertainty margin
  - Estimation method



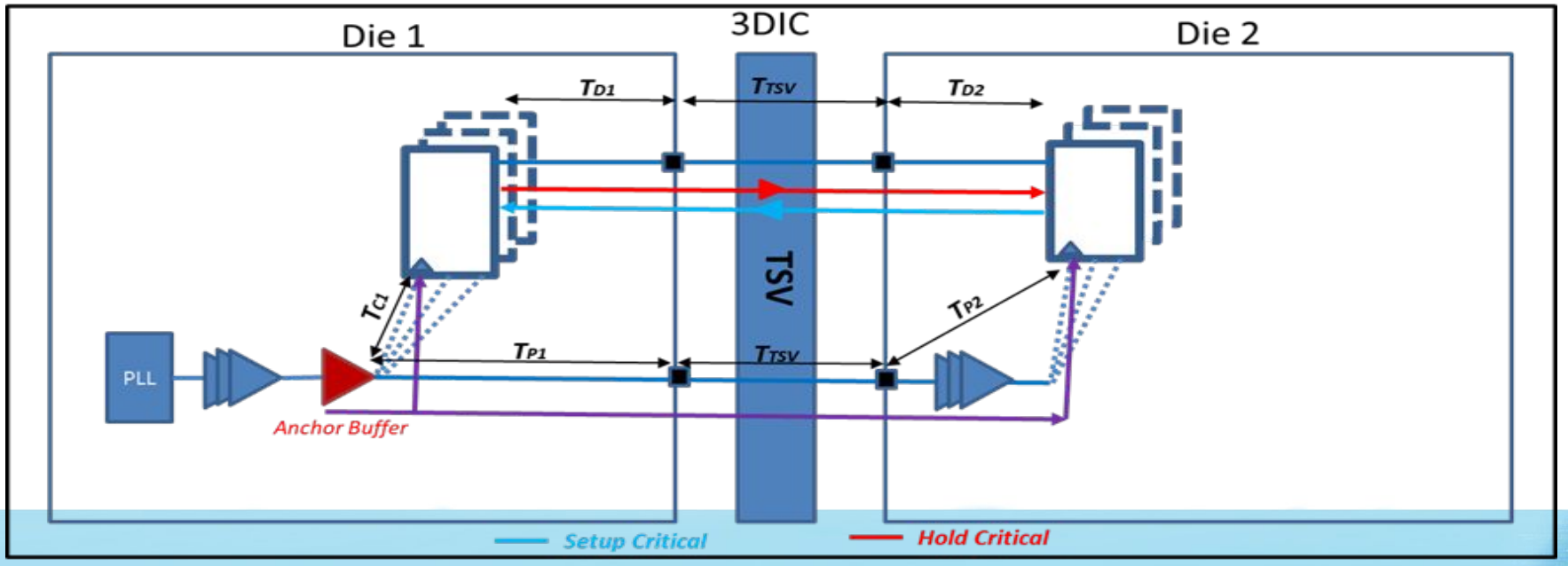


Path example

3DIC Sign-off Corner Reduction Method 3-1

- Setup equation $-T_{P1} - T_{TSV} - T_{P2} + T_{D2} + T_{TSV} + T_{D1} + T_{C1} \leq T_{Period} - T_{setup} - T_{Skew} - SUncern$

- Hold equation $T_{C1} + T_{D1} + T_{TSV} + T_{D2} \geq T_{P1} + T_{TSV} + T_{P2} + T_{Hold} + T_{Skew} + HUncern$



3DIC Sign-off Corner Reduction Method 3-1

- Scaling factor estimation
  - Voltage Scaling Factor(VSF)

$$VSF(SS_{Nom}) = Dealy(V_{Ref+\Delta}, SS_{Nom}) \,/\, Delay(V_{Ref-\Delta}, SS_{Nom})$$

$$VSF(FF_{Nom}) = Delay(V_{Ref-\Delta}, FF_{Nom}) \,/\, Dealy(V_{Ref+\Delta}, FF_{Nom})$$

  - Process Scaling Factor(PSF)

$$\text{PSF}(+\Delta) = Delay(V_{Ref+\Delta}, SS_{Nom}) \,/\, Dealy(V_{Ref+\Delta}, FF_{Nom})$$

$$\text{PSF}(-\Delta) = Delay(V_{Ref-\Delta}, SS_{Nom}) \,/\, Dealy(V_{Ref-\Delta}, FF_{Nom})$$

- Scaling

$$T_{D,+\Delta,SS,Nom} = T_{D,-\Delta,SS,Nom} \times VSF(\text{SS}_{\text{Nom}})$$

$$T_{D,+\Delta,FF,Nom} = T_{D,-\Delta,SS,Nom} \,/\, PSF(-\Delta)$$

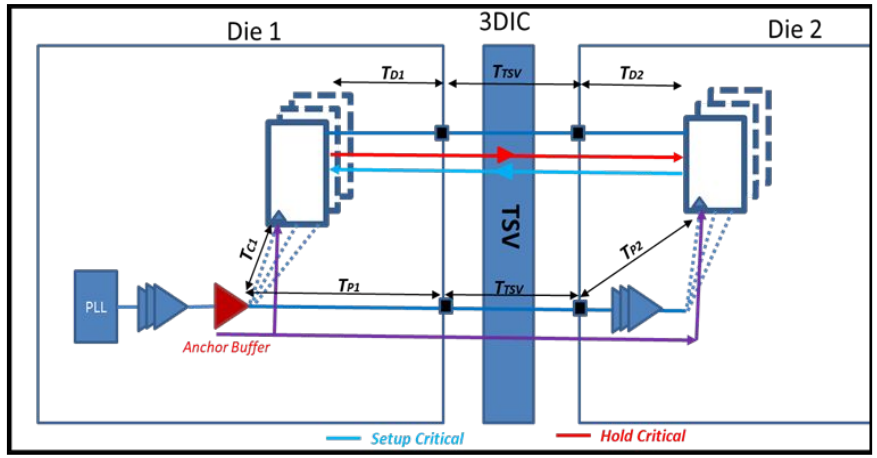
3DIC Sign-off Corner Reduction Method 3-4

- In early design stage, we can make more accurate budgeting
  - It can explore interface path with estimated path delay
- Example
  - Setup with voltage scaling

$$-(T_{P1} * VSF) - T_{TSV} - (T_{P2} * VSF) + (T_{D2} * VSF) + T_{TSV} + (T_{D1} * VSF) + (T_{C1} * VSF)$$
$$\leq T_{Period} - T_{setup} - T_{Skew} - SUncern$$

  - Hold with Process scaling

$$(T_{C1} * VSF) + (T_{D1} * VSF) + T_{TSV} + (T_{D2} * VSF)$$
$$\geq (T_{P1} * VSF) + T_{TSV} + (T_{P2} * VSF) + T_{Hold} + T_{Skew} + HUncern$$



Result & Discussion

- The interface analysis comparison between proposed vs. Full 3DIC analysis
  - Proposed runs separate sign-off for 3 parts
  - Interface timing sign-off meets all timing constraints.

	Full 3DIC timing analysis	Proposed (Die1 + Die2 + interface)	Reduction
Analysis corner	32	8	75%
CPU cores	32x8	8x8	75%
Peak memory	350G	30G	91%
STA runtime	18h	4h	78%

Conclusion

- 3DIC solution is expensive as sign-off aspect
  - To consider die to die variation, we should increase sign-off corners
- Using those methods, we can reduce TAT and computing resource

	Pros	Cons
Making asynchronous	Don’t need timing analysis	Need to change design scheme
Dominant corner sign-off method	Reducing corner dramatically	Need to analyze all corner at once
Budget based Sign-off	Simple method	Budgeting overhead
Budget based Sign-off with estimation	Reducing budgeting overhead	Need time to estimate delay